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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/187,197	11/03/1998	JACSON LIU	MVIP0005USA	2744

7590

04/23/2003

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EXAMINER

GUERRERO, MARIA F

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/187,197

Applicant(s)

LIU, JACSON

Examiner

Maria Guerrero

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 September 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 1998 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

1. This Office Action is in response to the Amendment filed September 10, 2002.

Claims 14-19 are canceled

Claims 1-13 are pending.

Election/Restrictions

2. Applicant's election without traverse of Group I (claims 1-13) in Paper No. 6 is acknowledged.

Drawings

3. Figures 1-6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 5-9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (U.S. 5,372,968) in view of Bose et al. (U.S. 5,492,858).

Lur et al. discloses forming a plurality of shallow trenches and generating at least one dummy on the trenches (Fig. 1-2, col. 3, lines 28-32). Lur et al. teaches forming trenches having different widths and the width of some trenches being greater than others (Fig. 2). Lur et al. shows forming a dielectric layer to fill the trenches and planarizing the structure to align the surface of the dielectric layer inside each trench with the surface of each component on the semiconductor wafer (Fig. 4-6, col. 3, lines 60-65). Lur et al. teaches the dummy being made of silicon and the dummy remaining covered by the dielectric material (Fig. 5-6). Lur et al. shows implanting into the substrate through the openings in the mask (col. 3, lines 50-55).

Lur et al. teaches forming a pad oxide layer on the substrate, forming a pad nitride layer on the pad oxide layer, and planarizing the structure by a first and a second planarization process (Fig. 1-5, col. 3, lines 15-30, 64-66, col. 4, lines 2-35).

Lur et al. does not specifically show condensing the dielectric layer by using an annealing process, the first planarization process being a polishing process. However, Bose et al. shows forming shallow trenches on a semiconductor substrate using photolithography and etching process (col. 4, lines 48-55). Bose et al. teaches filling the trenches employing TEOS and condensing the dielectric layer by using an annealing process (col. 5, lines 5-20). In addition, Bose et al. shows chemical mechanical polishing to planarize the surface (col. 5, lines 18-25) the width of the trenches being less than 2 microns (col. 4, lines 60-61), and performing a second planarization process (col. 5, lines 20-25).

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Regarding the specific width and height as claimed, the selection of any appropriated variable for a known process is within the capabilities of a person of ordinary skill in the art.

Since Lur et al. and Bose et al. are both from the same field of endeavor of forming trenches; the purpose disclosed by Lur et al. would have been recognized in the pertinent art of Bose et al.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Lur et al reference by including the teaching of Bose et al. in order to increase the etch resistant of the dielectric layer and to avoid recessing of the dielectric layer (Bose et al., col. 4, lines 4-8).

5. Claims 1, 4-5, 8, 10-11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkatesan et al. (U.S. 5,459,096) in view of Bose et al. (U.S. 5,492,858).

Venkatesan et al. discloses forming a plurality of shallow trenches and generating at least one dummy on the trenches (col. 5, lines 5-15). Venkatesan et al. teaches forming trenches having different widths and the width of some trenches being greater than others (Fig. 2). Venkatesan et al. shows forming a dielectric layer (TEOS) to fill the trenches (col. 5, lines 30-35). Venkatesan et al. discloses chemical mechanical polishing to planarize the surface in order to be aligned with the components (Fig. 6). Venkatesan et al. shows forming shallow trenches on a semiconductor substrate using photolithography and etching process (col. 5, lines 5-15). Venkatesan et al. shows

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performing a second planarization process to strip off (etching) the pad oxide layer and pad nitride layer from the surface (Fig. 7, col. 6, lines 40-45).

Venkatesan et al. does not specifically show condensing the dielectric layer by using an annealing process. However, Bose et al. teaches condensing the dielectric layer by using an annealing process as conventional in the art (col. 4, lines 4-10, col. 5, lines 14-15).

Since Venkatesan et al. and Bose et al. are both from the same field of endeavor of forming trenches, the purpose disclosed by Bose et al. would have been recognized in the pertinent art of Venkatesan et al.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Venkatesan et al reference by including the teaching of Bose et al. in order to increase the etch resistant of the dielectric layer and to avoid recessing of the dielectric layer (Bose et al., col. 4, lines 4-8).

Conclusion


6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gocho et al. (U.S. 5,498,565), Zdebel et al. (U.S. 5,004,703), Kim et al. (U.S. 5,677,232), Bashir et al. (U.S. 5,683,932), and Lur et al. (U.S. 5,308,786) teach forming teach having dummies. Jang et al. (U.S. 5,721,172) is cited as evidence to show that the selection of any appropriated width and height for a known process is within the capabilities of a person of ordinary skill in the art.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 703-305-0162.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


Maria Guerrero
Patent examiner
April 18, 2003